REMARKS

Reconsideration of the application is respectfully requested.

The following discussion addresses the issues in the order in which they have been raised in the Office Action.

Drawings

As requested in the Office Action, Fig. 10 has been added to show the features specified in claims 4 and 5, without introducing any new matter.

Applicants have also added a brief description of Fig. 10, as well as references to Fig. 10 in the Detailed Description section as appropriate.

Claim Objections

The objections to claims 17 and 21 have been noted and addressed in this amendment.

Claims Rejected Under 35 U.S.C. §112

This amendment also addresses the potential indefiniteness pointed out with respect to certain language in claims 1, 9, 11, 17-18, and 20.

Claims Rejected Under 35 U.S.C. §103

Claims 1-3 and 6-21 stand rejected as being not patentable under 35 U.S.C. §103(a) in view of "PCI Express Base Specification Revision 1.9" ("Base Spec"), in view of U.S. Patent No. 7,127,648 to Jiang, et al. ("Jiang"). Applicants respectfully disagree with the rejection for the following reasons.

At page 7 of the Office Action, it is held that Base Spec teaches Applicants' method recited in claim 1, and in particular, the operations of *programming a plurality of registers of the IC device to set a test symbol data pattern and configure a lane transmitter of the link; and programming a start bit in the register of the IC device to request that the IC device be placed in a measurement mode.* Specifically, the Office Action points to Sections 4.2.1 and

4.2.8 of <u>Base Spec</u>, as allegedly teaching the limitation of *programming the registers to set a test symbol data pattern*. However, those sections of <u>Base Spec</u> do not reasonably provide any such teaching. Section 4.2.1 describes symbol encoding and, in particular, the scheme used in PCI Express referred to as 8b/10b transmission code. This describes how an input 8 bit character is mapped to a 10 bit symbol for transmission (and how the reverse occurs during reception). There is nothing about *programming a register of an IC device to set a test symbol data pattern*.

The Office Action, also at page 7, points to Section 4.2.5.3 of <u>Base Spec</u> as allegedly teaching Applicants' claimed limitation *programming a register of the IC device to configure a lane transmitter for the link*. Here it is instructive to refer to, for example, paragraph [0036] of Applicants' Specification as filed, which describes an example how the link transmitter may be configured with certain signaling formats. The Office Action finds that the language *programming a register of an IC device to configure a lane transmitter for the link* is reasonably taught in Section 4.2.5.3 of <u>Base Spec</u>, which describes a particular state of a link state machine in a PCI Express compatible IC device. In this state (referred to as "Configuration"), both the transmitter and receiver of the device are sending and receiving data at a particular rate. It is said that the link "configures width and lane reversal, and manages lane-to-lane skew within the link." This self configuration may be automatically negotiated between the two ends of the link. However, this does not teach or suggest that *a transmitter for the link (in the IC device) be configured while programming one or more registers of the IC device*.

As to Applicants' further limitation of *programming a start bit in a register of the IC device to request that the link be placed in a measurement mode*, the Office Action points to a "MSI enable bit" as seen in Fig. 7-8 of <u>Base Spec</u>. However, the <u>Base Spec</u> enclosures provided with the Office Action only include a single page with Fig. 7-8. There is no textual description that may assist in verifying the meaning of the term "MSI" and whether it refers to a measurement mode (as this mode is further described in Applicants' claim 1). Accordingly, it is respectfully submitted that the Office Action does not make a sufficient case for rejecting claim 1 as being obvious in view of <u>Base Spec</u>. As <u>Jiang</u> also fails to provide the missing teachings mentioned above, it is respectfully requested that the rejection in view of <u>Base Spec</u> and <u>Jiang</u> be withdrawn.

As to claim 9, this claim is rejected as being obvious in view of Jiang and Base Spec, as explained on pages 9 and 10 of the Office Action. However, neither Jiang nor Base Spec teach or suggest that *the IC device is to enter a measurement mode from a normal mode, in response to a predefined bit of a register of the IC device being programmed, where there are one or more programmable registers in the IC device whose bits instruct the measurement mode circuitry to change a data pattern in the sequence of test symbols that is transmitted over the link while the link is operating in the measurement mode, and change an autoinvert setting, a default setting for an inverted lane, an inversion setting, and initial disparity for the link.* With all due respect, the Office Action again makes an insufficient showing as to why Jiang would be able to reasonably teach or suggest to one or ordinary skill in the art such limitations. The Office Action only points to Fig. 6 of Jiang, and in particular, a digital core 625c that includes a packet generator and a packet checker. These are part of a chip's built-in self-test capability. However, that general terminology is insufficient to teach or suggest the specific limitations recited in Applicants' claim 9 regarding the actions taken by the IC device in response to registers being programmed. The Office Action again points to the MSI enable bit in Fig. 7-8 of Base Spec, as allegedly teaching that a link can enter measurement mode from a normal mode in response to a predefined bit of a register (in an IC device coupled to the link) being programmed. It is respectfully requested that the Examiner provide additional textual description of the MSI enable bit.

Lastly, the Office Action points to Table 5-6 of Base Spec as teaching programmable registers. However, that Table only describes a bridge control register whose programmable bits are not associated with any testing or measurement activities including *changing data patterns in a sequence of test symbols and lane transmitter configurations including autoinvert setting, default setting, inversion setting, or initial disparity* (as required by Applicants' claim 9). Therefore, reconsideration and withdrawal of the rejection of claim 9 is respectfully requested.

As to independent claim 17, this claim contains some limitations that are similar to those argued above in connection with claim 9, such that claim 17 is also submitted as not being obvious for at least the same reasons given in support of claim 9.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious, for at least the same reasons given above in support of their base claims.

It should be noted that not all of the assertions made in the Office Action, particularly those with respect to the dependent claims, have been addressed here, in the interest of conciseness. Applicants reserve the right to challenge any of the assertions made in the Office Action by the Examiner, with respect to the relied upon art references and how they would relate to Applicants' claim language, including the right to swear behind or otherwise remove an improper art reference.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending patentably define the subject invention over the prior art of record and are in condition for allowance and such action is earnestly solicited at the earliest possible date.
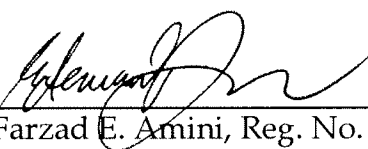
If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly extension of time fees.

Respectfully submitted,

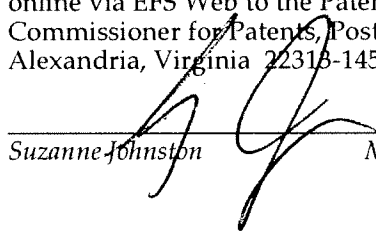BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: May 13, 2008.   By _____

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Suzanne Johnston   May 13, 2008